WHAT IS CLAIMED IS:

1. An IC card supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, and including an input-output operation of data with an encoding process or a decoding process executed by an encoding processing computing unit operated in response to instructions issued from a central processing unit,

wherein said encoding processing computing unit is provided with each of registers, which stores data used for a computation for the encoding process or decoding process in plural bit units, and data necessary prior to the encoding process or the decoding process is stored in the register.

2. The IC card according to claim 1, wherein said encoding process or decoding process includes an exponential residue multiplying operation applicable to RSA cryptography or the like, and

said encoding processing computing unit alternately computes $A = A^2 \text{ mod} N$ and $A = AB \text{mod} N$ with $A = 1$ and $B = X$ in response to X, Y and N inputted thereto, computes $A = A^2 \text{ mod} N$ corresponding to plural bits as viewed by plural bits from a high order of Y upon said computation, and brings the value of B necessary for the computation of ABmodN from the register in association with combinations

of the plural bits.

3. An IC card supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, and including an input-output operation of data with an encoding process or a decoding process executed by an encoding processing computing unit operated in response to instructions issued from a central processing unit,

wherein said encoding processing computing unit has a signal path for capturing data used for the next computation from a storage circuit concurrently with a computing operation for the encoding process or decoding process.

4. The IC card according to claim 3, wherein said encoding process or decoding process includes an exponential residue multiplying operation applicable to RSA cryptography or the like, and

said encoding processing computing unit alternately computes $A = A^2 \bmod N$ and $A = AB \bmod N$ with A = 1 and B = X in response to X, Y and N inputted thereto, computes $A = A^2 \bmod N$ corresponding to plural bits as viewed by plural bits from a high order of Y upon said computation, and brings the value of B necessary for the computation of $AB \bmod N$ corresponding to combinations of the plural bits from the storage circuit concurrently with said

computation of A^2 modN.

5. An IC card, which is supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, in which a central processing unit, a storage circuit, an encoding processing computing unit and a random number generator are connected to a common address bus, and which includes an input-output operation of data with an encoding process or a decoding process executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

wherein said central processing unit supplies a leading address at which data for the encoding or decoding process is stored, to the storage circuit, and said storage circuit reads data, based on an address signal formed by a built-in address generating circuit based on the leading address and transfers the same to the encoding processing computing unit, and each of random numbers produced by the random number generator is transmitted to an address bus commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.

6. The IC card according to claim 5, wherein said

encoding process or decoding process includes an exponential residue multiplying operation applicable to RSA cryptography or the like, and

said encoding processing computing unit alternately computes $A = A^2$ modN and $A = AB$modN with $A = 1$ and $B = X$ in response to X, Y and N inputted thereto, computes $A = A^2$ modN corresponding to plural bits as viewed by plural bits from a high order of Y upon said computation, and brings the value of B necessary for the computation of ABmodN from the storage circuit in association with combinations of the plural bits.

7. An IC card, which is supplied with an operating voltage by an electrical connection between each of external terminals and a read/write device, in which a central processing unit, a storage circuit, an encoding processing computing unit and a random number generator are connected to a common address bus, and which includes an input-output operation of data with an encoding process or a decoding process executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

wherein said central processing unit supplies an encoded address signal formed using each of random numbers produced by the random number generator to the storage circuit, which decodes the address signal through

the use of the random number to generate a leading address,

said storage circuit reads data for the encoding process or decoding process, based on the address signal produced by a built-in address generating circuit on the basis of the leading address and transfers the same to the encoding processing computing unit, and

each of the random numbers produced by the random number generator is transmitted to the address bus commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.

8. The IC card according to claim 7, wherein said encoding process or decoding process includes an exponential residue multiplying operation applicable to RSA cryptography or the like, and

said encoding processing computing unit alternately computes $A = A^2$ modN and A = ABmodN with A = 1 and B = X in response to X, Y and N inputted thereto, computes $A = A^2$ modN corresponding to plural bits as viewed by plural bits from a high order of Y upon said computation, and brings the value of B necessary for the computation of ABmodN from the storage circuit in association with combinations of the plural bits.

9. A microcomputer having a module configuration including an input-output operation of data with an encoding process or a decoding process executed by an encoding processing computing unit operated in response to instructions given from a central processing unit,

wherein said encoding processing computing unit is provided with each of registers, which stores data used for a computation for the encoding process or decoding process in plural bit units, and data necessary prior to the encoding process or the decoding process is stored in the register.

10. The microcomputer according to claim 9, wherein said module configuration is formed on one semiconductor substrate for the implementation thereof.

11. A microcomputer having a module configuration including an input-output operation of data with an encoding process or a decoding process executed by an encoding processing computing unit operated in response to instructions issued from a central processing unit,

wherein said encoding processing computing unit has a signal path for capturing data used for the next computation from a storage circuit concurrently with a computing operation for the encoding process or decoding process.

12. A microcomputer having a module configuration in which a central processing unit, a storage circuit, an encoding processing computing unit and a random number generator are connected to a common address bus, and which includes an input-output operation of data with an encoding process or a decoding process executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

wherein said central processing unit supplies a leading address at which data for the encoding or decoding process is stored, to the storage circuit,

said storage circuit reads data, based on an address signal formed by a built-in address generating circuit based on the leading address and transfers the data to the encoding processing computing unit, and

said random number generator transmits each of produced random numbers to an address bus commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.

13. A microcomputer having a module configuration in which a central processing unit, a storage circuit, an encoding processing computing unit and a random number generator are connected to a common address bus, and

which includes an input-output operation of data with an encoding process or a decoding process executed by the encoding processing computing unit and the storage circuit operated in response to instructions given from the central processing unit,

wherein said central processing unit supplies an encoded address signal formed using each of random numbers produced by the random number generator, to the storage circuit,

said storage circuit decodes the encoded address signal supplied from the central processing unit by using the random number to thereby generate a leading address, reads data for the encoding or decoding process and transfers the data to the encoding processing computing unit, and

said random number circuit transmits the produced random number to the address bus commonly connected with the central processing unit, the storage circuit and the encoding processing computing unit as a pseudo address signal in association with the data transfer.